Software Reconfigurable Baseband ASSP for Dual Mode UMTS/WLAN 802.11b Receiver

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ABSTRACT

In this paper, an application specific signal processor (ASSP) for dual mode baseband processing of UMTS and WLAN 802.11b signals is presented. Although both mobile communication standards are based on direct sequence spread spectrum (DS-SS) technology, there are substantial differences in the signal processing algorithms that have to be realized. For this reason, the presented approach is mainly based on a flexible DSP architecture on which the signal processing algorithms are implemented by means of software. Within the paper, the proposed hardware architecture is presented. Furthermore, the results of the software implementation, as well as the results of VHDL synthesis are discussed.

I. INTRODUCTION

The wireless infrastructure tends to be more and more heterogeneous. There are many wireless standards and systems providing various services to the mobile user. Depending on the coverage area of the wireless network, there exist either local area wireless systems like IrDA, DECT, WLAN, Bluetooth, Hiperlan/2, or global cellular systems GSM, UMTS, IMT2000. To maximally utilize the deployed wireless environment, interoperability will be the key feature of the next generation of mobile terminals. Multistandard modems will be implemented into the terminals, to be capable of operating in various wireless networks.

3G UMTS cellular networks are designed to provide voice and data services with high user mobility and wide area coverage. On the other hand, wireless LANs, such as IEEE 802.11b, offer higher data rates in local areas with restricted mobility. The combination of high data rates of WLAN and the ubiquity of UMTS networks is very attractive for the user. The main motivation of this work is the efficient integration of the baseband processing of both standards in the mobile terminal.

This paper proposes a programmable hardware architecture for UMTS and WLAN baseband processing. The modem realizes the basic physical layer functionality of UMTS/W-CDMA downlink and WLAN 802.11b standard, namely synchronization, signal despreading, and demodulation. Instead of using separate hardware for each standard, we prefer the implementation on a common hardware platform.

In the following section 2, an overview of UMTS and IEEE 802.11b standard is given. The core algorithms of typical receiver structures are briefly explained. In section 3, our approach of a programmable dual mode hardware architecture is presented. Finally, the results are summarized and discussed.

II. CORE ALGORITHMS OF UMTS AND 802.11B

A. UMTS

The Universal Telecommunication Standard System (UMTS) is based on DS-CDMA technology. I.e., the data spectrum of the transmit information signal is spread by multiplication with a specific pseudonoise (PN) sequence. Different channels are separated by using different PN sequences, thus allowing for code division multiple access (CDMA).

In UMTS [1], the symbols to be sent are QPSK modulated. The spreading sequence is constructed from a channelization code and a scrambling code. In downlink transmission, the channelization code is used to separate different users of one base station, as well as to realize different spreading factors (orthogonal variable spreading factor code – OVSF code), and thus, different data rates. The scrambling codes are cell specific and identical for the users of one cell. For frequency division duplex (FDD) mode, a long scrambling code with period of 38400 chips has been specified. The basic parameters of the UMTS system are summarized in Table 1.

Parameter	Value
Spreading factor	{4,8,16,32,64,128,256,512}
Chip rate	3.84 Mcps
Carrier frequency	Approx. 2 GHz
Roll-off factor	0.22
Bandwidth	5 MHz
Frame length	10ms (38400 chips)
Slot length	2560 chips
Slots per frame	15
Modulation	QPSK

Table 1: System parameter set for 3GPP FDD mode

The commonly used receiver type for DS-SS systems is the Rake receiver [7]. It can be seen as a special implementation of a matched filter (MF) receiver. The Rake receiver despreads the received signals corresponding to different multipath components of the mobile radio channel separately. Subsequently, the despread signal components are combined together to obtain the symbol estimates, i.e., the phase corrected, and time aligned signals are added together. It shall be noted that channel estimation is necessary in order to estimate the phase of each received multipath component. Furthermore, due to the continuous signal transmission, a time-tracking is needed.
The most important tasks to be carried out by the receiver are summarized below:

- Initial timing synchronization (acquisition)
- Signal despreading, i.e., multiplication of the received signal with the conjugate complex and synchronized copy of the PN sequence
- Channel estimation and time-tracking
- Combining and detection

B. WLAN 802.11B

IEEE 802.11b standard [2,3] specifies a DS-SS WLAN system providing wireless data transmission with rates ranging from 1 to 11 Mbps in the 2.4 GHz ISM band. The 802.11b standard employs asynchronous packet transmission with time division duplex (TDD). Each data packet (PPDU) consists of a preamble, header and data part (PSDU). To realize different data rates, the PSDU uses different modulation schemes, namely DBPSK/DQPSK with Barker spreading for 1/2 Mbps (Low rate modes), or CCK (Complementary Code Keying) modulation for 5.5 and 11 Mbps (High rate modes) transmission. The basic parameters of the WLAN 802.11b system are summarized in Table 2.

Parameter	**Preamble/ Header**	**PSDU**
Spreading Factor	11 (Barker code)	1/2 Mbit: 11 (Barker) 5.5/11Mbit: 2/1 (CCK)
Chip rate	11 Mcps	
Carrier frequency	2.4 GHz	
Frame length	144 bit/48 bit	Variable
Modulation	DBPSK	1 Mbit: DBPSK 2 Mbit: DQPSK 5.5 Mbit: 4-CCK 11 Mbit : 64-CCK

Table 2: System parameters of WLAN 802.11b mode

In principle both, a matched filter based receiver or an equalizer based receiver are suited for demodulation/detection of WLAN 802.11b signals. To avoid separate demodulation within each Rake finger, which is quite complex in case of CCK demodulation, the Rake receiver can also be employed, when it is modified in the appropriate way, such that first the channel matched filter operation is carried out followed by DBPSK/DQPSK or CCK demodulation.
The most important tasks to be carried out for WLAN 802.11b demodulation/detection are given below:

- Initial timing synchronization (acquisition) based on the preamble.
- Demodulation, detection, and bit descrambling of the header (header information required for PSDU processing).
- Demodulation, detection, and bit descrambling of the PSDU, i.e. Barker despreading and DBPSK/DQPSK demodulation in 1/2 Mbps mode and 4/64 CCK demodulation in 5.5/11 Mbps mode

It shall be noted that time tracking not necessarily has to be done, as it can be assumed that timing drift is negligible for one packet duration. Furthermore, due to differential modulation non-coherent demodulation can be used. Thus, no phase estimation is required [7].

III. HARDWARE DESIGN

We start the design of our hardware architecture by the analysis of baseband receiver algorithms from computational complexity point of view. The receiver tasks can be divided into:

- Acquisition,
- Despreading and demodulation,
- Other algorithms like control algorithms, channel estimation, time-tracking, bit descrambling, etc.

The computational requirements of individual tasks for the dual mode baseband modem are summarized in Table 3. It is evident that the most critical task with respect to the computational complexity is the signal acquisition. On the other hand, WLAN High rate mode requires the most complex demodulation algorithm.

Task	Computational effort [MOPS]		
	UMTS	WLAN Low rate	WLAN High rate
Acquisition	2000	5800	5800
Demodulation	50 / finger	250	700

Table 3: Computational requirements of essential receiver tasks. It is assumed, the UMTS and WLAN input baseband signals are 4 and 2 times oversampled i.e. sample frequencies are 15.36 MHz and 22 MHz, respectively.

The initial timing synchronization (acquisition) for both standards can be implemented similarly by the use of a filter matched to a known training sequence with subsequent peak detection. Due to the high computational complexity of this task, it has been decided to implement a dedicated configurable hardware for it.

The algorithms for demodulation/detection of both standards differ significantly, although both standards are DS-SS based. Hence, a programmable architecture is the preferable solution for the demodulation task.
All other algorithms, such as control algorithms and channel estimation, are different for UMTS and WLAN 802.11b. Therefore an implementation on a programmable architecture is preferable.
In addition, because of the demonstrative character of this work, the basic functionality has been implemented in our design with the following simplifications:

- simplified CPICH based acquisition for UMTS, i.e. it is assumed, the cell specific scrambling code is known to the receiver,
- only one RAKE finger was implemented, the extension is possible with moderate effort,
- channel estimation and time tracking implemented for UMTS only,
- only long PPDU preamble/header format supported in WLAN mode,
- noncoherent demodulation of differential BPSK/QPSK in WLAN mode implemented only (easy extension to coherent demodulation by minor software changes possible)

By summing up previous considerations, the proposed dual mode receiver architecture consists of:

- dedicated configurable acquisition unit,
- programmable DSP processor.

The block diagram of the proposed receiver hardware architecture is shown in Figure 1.
The acquisition unit consists of a matched filter, a trigger unit, an address generation unit (AGU) and a store unit. Depending on the mode of operation to be selected (UMTS/WLAN Low rate/WLAN High rate), the matched filter performs a sliding correlation of the input data with a known code sequence (preamble code segment in WLAN 802.11b mode or CPICH code segment in UMTS mode). The filter coefficients are initialized during the processor initialization process via a control interface. Initial timing synchronization is achieved by detecting an output peak of the matched filter in the trigger unit In order to avoid frequent false alarms, the output peaks are subject to an advanced threshold test. I.e. a first threshold crossing defines the start of a search window with predefined length. Within the search window the strongest peak is determined. If the selected peak exceeds a second threshold, timing synchronization is declared as the timing instant corresponding to this peak.
When a valid peak has been detected, the samples of the received signal are written into the FIFO buffer of the DSP processor. This operation starts with a predefined delay which is given by an external control register. The memory addresses for FIFO buffer write operation are generated by the acquisition AGU unit; and the Store Unit selects the desired input samples from the input data stream to be written into the FIFO buffer. Three different memory write modes are distinguished: UMTS mode, WLAN Low Rate Mode (1 and 2 MBps), and WLAN High Rate Mode (5.5 and 11 MBps). It is noted, that for WLAN High rate burst processing switching between the Low Rate and High Rate Memory write modes is required, since the header of a WLAN burst is always transmitted with a rate of 1 Mbps.
The DSP processor itself is application specific, i.e., it is designed to effectively map the baseband algorithms of the three different modes. It is based on the synchronous transfer architecture (STA) [4].
The DSP consists of a vector processing unit and a scalar processing unit. The Vector processing unit has 16 parallel data paths (slices) which are controlled according to the SIMD principle (single instruction multiple data). All data manipulation operations are performed by the vector processing unit. The basic processing bit width is 16 bit. The structure of a single slice is illustrated in Figure 2. Each slice contains an ALU, a Barrel shifter, a multiplier, 4 input registers, and 4 accumulator registers. The vector processing unit has read/write access to the block data memory. The block data memory has a reserved area into which the input FIFO buffer is mapped. Besides, there is

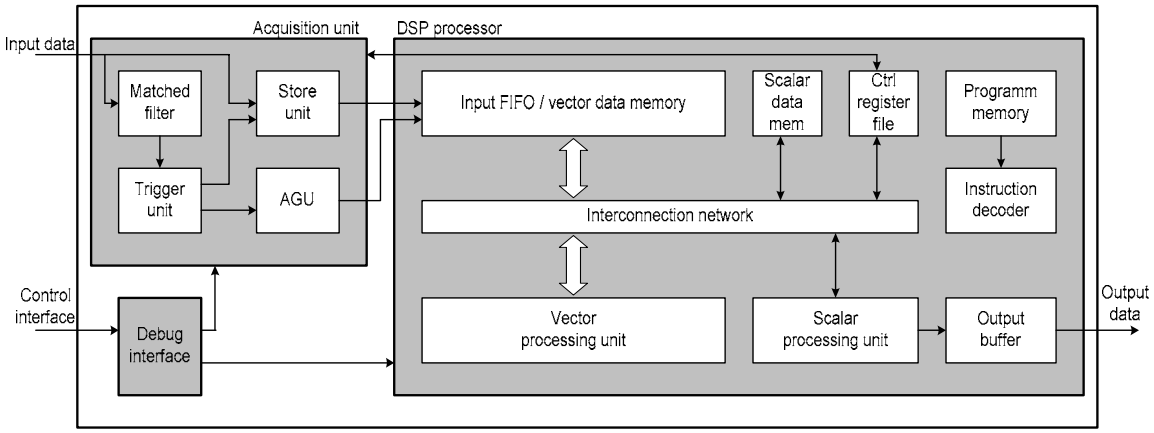

Figure 1: Block schema of dual mode UMTS/WLAN baseband processor. Note, that two independent parallel interconnection units are represented by block interconnection network.

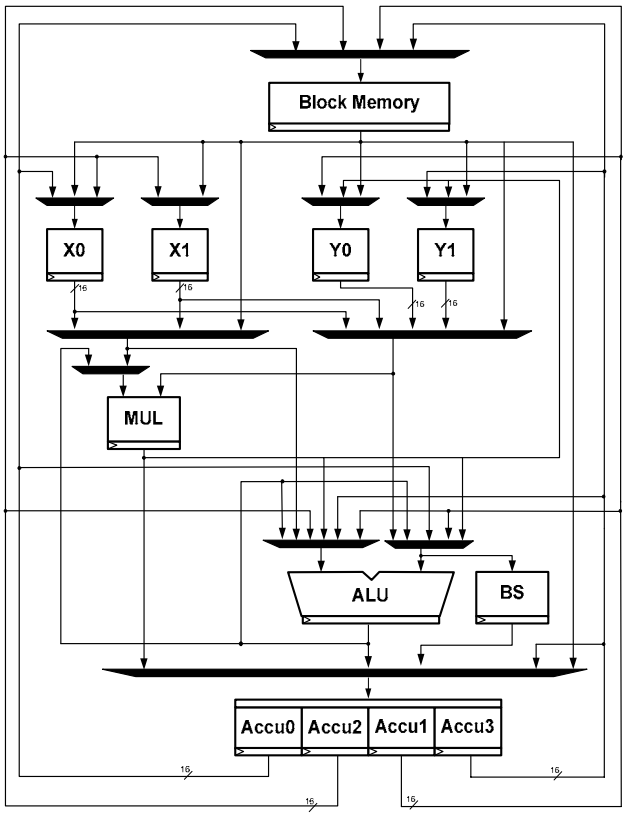

Figure 2: Block diagram of a single datapath (without ICU connections)

additional memory space that can be used arbitrarily by the vector processing unit. In order to allow for data transfers between slices, as well as data transfer between vector and scalar processing unit, two independent interconnection units (ICU) exist. Each ICU allows for certain data exchange operations, like data broadcast and special butterfly transfers, as required by CCK demodulation.
The scalar processing unit performs the address generation for all data memories and is used for scalar data manipulations as well. It is connected to two scalar memories. It also controls the acquisition unit by a control register file.

Mode	# slices
UMTS	4 per RAKE finger
WLAN low rate - preamble/PPDU	1
WLAN high rate – preamble	1
WLAN high rate – PPDU	16

Table 4: Slice allocation of vector processing unit

It shall be noted that each slice of the vector processor can be activated or deactivated separately by a slice enable mechanism which is controlled via a slice enable register that can be set by the scalar processing unit. Thus power can be saved, if not all slices are needed for processing. For example, Table 4 illustrates the slice usage of the implemented baseband demodulation for the different operation modes. On the other hand, the slice enable mechanism provides the possibility to implement algorithms that are not well suited for SIMD processing, such as inter-slice sorting algorithms.

IV. RESULTS

A. VHDL SIMULATION

The behavior of the VHDL implementation has been tested by means of simulations for UMTS and WLAN 802.11b baseband signal processing. Test signals have been generated and bit error rates have been measured under consideration of AWGN distortion. The results have been compared to those obtained with a reference MATLAB implementation. The comparison showed almost identical performance. Besides, the performance in terms of required cycles has been characterized. For example, Table 5 illustrates the cycle budget for the UMTS demodulation tasks on a frame basis (10 ms). Except for the first (and most complex) operation all others depend on system parameters such as spreading factor and lengths of estimation intervals. It should be noted, that the required cycles are not distributed equally over all chips. Therefore some buffering of the input data or an increased clock rate is necessary to compensate for the delays in case of 'high complexity' chips.

Subtask	# of Cycles
Despreading & accumulation	691.200 / frame
Detection and demodulation of DPCH	144.000 / frame
Computation of channel estimation and time-tracking error signal	2420 / frame
Processing of output bit register	7200 / frame
Other (counter, loop init)	266 / frame
Σ	**845.086** / frame

Table 5: Cycle Count for UMTS demodulation (the numbers refer to our implementation) over 1 frame (1 ms) with spreading factor 4 and estimation interval length of one slot for both channel estimation and time-tracking error signal

To illustrate the WLAN 802.11b cycle requirements of our implementation, the 11 Mbps CCK demodulation is taken as an example. Table 6 summarizes the number of cycles required by the several tasks for 11 Mbps CCK demodulation. It shall be noted that with our implementation 4 CCK symbols are processed in parallel, i.e. with the 16 data path SIMD architecture, processing of one symbol is distributed among 4 data paths. Furthermore the bit descrambling operation as required by the WLAN 802.11b standard is completely performed on the scalar processing unit. Hence, descrambling can be carried out in parallel to the CCK demodulation without increasing the total number of cycles (for this reason the number of cycles for the despreading operation is given in brackets in Table 6). Taking into account the sampling rates of UMTS and

WLAN 802.11b, it can be concluded that the requirements of the WLAN system are stronger and have to be regarded for the design. From its cycle requirements it follows that real time processing requires a processor clock of 100 MHz.

Subtask	# of Cycles
Sign correction input data	14 / 4 symbols
CCK-Correlation	102 / 4 symbols
$\|.\|^2$ + Max search within slices	122 / 4 symbols
Max search between 4 successive slices	34 / 4 symbols
DQPSK Demodulation	11 / 4 symbols
(Bit Descrambling)	(24) / 4 symbols
Σ	**283+(24)** / 4 symbols

Table 6: Cycle Count for WLAN 802.11b 11 Mbps demodulation (the numbers refer to our implementation, which processes 4 CCK symbols in parallel)

B. VHDL SYNTHESIS

For the estimation of chip area and timing requirements the processor has been synthesized with the Synopsys Design Compiler using the 0.13um library by UMC. The resulting area requirements and equivalent gate counts (without memories) are summarized in Table 7. To achieve the projected minimal clock speed of 100MHz mentioned before, synthesis time constraints 200MHz have been used. This time constraints have been met in the synthesis.

UNIT	AREA [μm^2]	AREA [%]	# of gates [2 input NAND]
Acquisition Unit	1,059,492	58.2 %	204,377
- matched filter	1,046,098	57.5 %	201,793
- agu	4,307	0.2 %	831
- trigger unit	8,861	0.5 %	1,709
- store unit	224	0.0 %	43
DSP processor	760,190	41.8 %	146,662
- scalar unit	52,604	2.9 %	10,147
- slice of vector unit	39,989	2.2 %	7,714
- ICU network	49,481	2.7 %	9,545
- control	18,257	1.0 %	3,525
Total	1,819,682	100%	351,019

Table 7: Area requirements of some design units

V. CONCLUSIONS

In this paper we presented hardware architecture of dual mode UMTS/IEEE802.11b baseband receiver providing real time baseband signal processing at 100 MHz processor clock. This architecture is based on a configurable dedicated acquisition unit and programmable DSP processor for demodulation and control.

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