CATS @ Vodafone Chair

SAMIRA

Matlab – Processor

Low Power. High Performance.

Samira is the first silicion version of processors based on the STA architecture template. STA (synchronous transfer architecture) is a novel DSP architecture featuring SIMD & compressed VLIW. A minimized control overhead in combination with sufficient computational resources enables low power, yet high performance processing. Degress of freedom for registers, memories, functional units, operations, parallelism provide design flexibility and enable tailored designs. The compiler-friendly architecture allows for automatic generation of code, core, binutils, testbenches and testpatterns. In short:
A multilevel design exploration with silicon protoyping becomes feasible.

Features

32Bit single-precision floating point DSP with 8 parallel data paths. 4.275 GFLOPs or 2G FPMAC/s @ 250Mhz. 100kb on-chip SRAM. Area: 10mm² with UMC 0.13µm. Wishbone compliant interface. Tape-out targeted for December 2004.

Scalar Unit

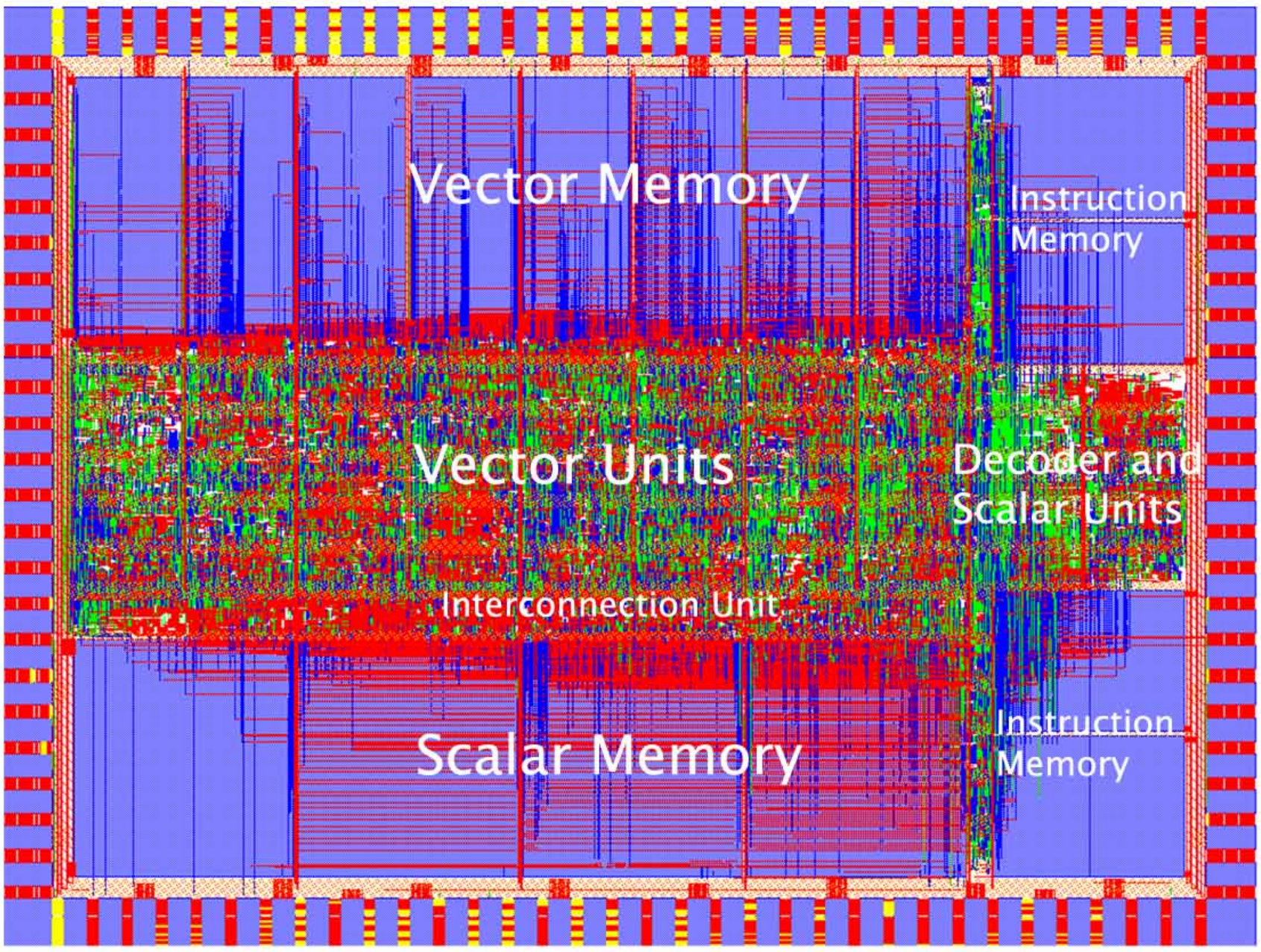
1 Floating Point Unit
4 ALUs
Multiplier
Barrel-Shifter
Sequencer
Register File
Memory

Address computations,
Program control and
non-vectorizable algrotihms

Vector Units

16 Floating Point Units
8 ALUs
8 Barrel-Shifter
Register File
Memory

Number crunching of
vectorizable algorithms



Dr. Gordon Cichon
Processor-Architecture and Compiler Design

Jie Guo
Compiler Optimization

Torsten Limberg
Module Design and Backend

Dr. Emil Matus
Floating Point Units and Numeric

Pablo Robelly
Tensor Compiler and Algorithm Design

Hendrik Seidel
Verification and Integration